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Patentanmeldung Nr. | **Patent application No.** | **Demande de brevet n°**

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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Receiver and sigma delta modulator for use therein

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Receiver and ΣΔ-modulator for use therein

The invention relates to a receiver comprising means for receiving a plurality of communication channels, a mixer for frequency-converting at least part of said communication channels and a sigma-delta modulator for analog to digital converting output signals of the mixer, said sigma-delta modulator including a feedback loop with a forward path and a feedback path, wherein the forward path comprises combiner means with a first input receiving the mixer output signals, noise-shaping low pass filtering means coupled to the output of said combiner means and a quantizer coupled to the output of the noise-shaping low pass filtering means and wherein the feedback path is connected to supply output signals of the quantizer to a second input of the combiner means.

A receiver of the abovementioned kind is e.g. known from the article "A 10.7-MHz IF-to-Baseband ΣΔ A/D Conversion System for AM/FM Radio Receivers" of E.J. van der Zwan et al in IEEE Journal of Solid State Circuits, Vol. 35, No 12, December 2000.

The above referenced known receiver comprises between the mixer output and the input of the sigma delta modulator a low-pass or band-pass filter for passing the desired communication channel and for suppressing the undesired neighboring channel(s). A great disadvantage of this kind of receivers is that severe requirements are to be set to the channel filter. The filter should add a minimum amount of noise and signal distortion and it should be of sufficiently high order to suppress the neighboring interferers. In order to avoid these disadvantages of the channel filter prior to the analog to digital conversion, a more popular approach is to place the channel filtering function in the digital domain after the analog to digital converter. In this concept use is made of the fact that digital filtering can nowadays be performed more economically and accurately than analog filtering. However, one disadvantage thereof is that the sample rate of the analog to digital conversion should be high enough to avoid aliasing of the interferers into the desired channel. A second disadvantage is that the dynamic range of the analog to digital converter has to be very large (e.g. 100 dB), inter alias because the interferers in the output of the mixer may have levels that are far greater than the level of the desired channel. The consequence is that in the analog to digital

converter and in the digital circuitry thereafter the sample rate and/or the number of bits per sample have to be chosen very large. The power consumption of the AD-converter and the digital circuitry thereafter will therefore be large. Moreover non-linear distortion in the AD-converter may easily occur. In order to make the disadvantages of the prior art receiver more acceptable, the abovementioned document also proposes to have part of the channel filtering before the AD-converter and the other part of the channel filtering behind the AD-converter.

It is the primary object of the present invention to substantially mitigate the fore mentioned problems of the prior art receivers and the receiver according to the invention is therefore characterized in that the forward path and the feedback path are so arranged that the signal transfer function of the ΣΔ-modulator from the input of the combiner to the output of the quantizer has a pass band that substantially corresponds with the frequency band of the communication channel to be filtered while the interferers beyond that pass band are attenuated. A major objective of the invention is that the channel selection filtering can be much simpler implemented within the loop of the ΣΔ-modulator then when this filtering would be done in front of this loop. The channel filtering has to prevent that large interferers in the neighborhood of the desired channel over-load the ΣΔ modulator and this may be implemented far easier and with lower noise factor in the loop filter behind the combiner where the signals are substantially reduced with respect to the signals in front of the combiner. The usually rather small signal to noise ratio that is required for the digital post-processing can now easily be obtained by a low order single-bit analog ΣΔ converter with low oversampling also because the digital decimation filter that usually follows the ΣΔ-modulator further suppresses remnants of the neighbor-channels. Moreover an advantage of a single bit ΣΔ converter is that for the quantizer a simple one-level comparator can be used and the digital to analog converter in the feedback path between the comparator and the input-combiner can then often be simplified.

It is quite possible in an arrangement according to the invention to combine the noise shaping function and the channel filtering function in a single filter arrangement. An example thereof will be given in fig. 1 of the present application. However preferably the filter means for the channel filtering and those for the noise shaping are separated, so that they each may be optimized independently from each other. An example of a receiver with such implementation is characterized in that the forward path of the feedback loop comprises, in addition to said noise shaping low pass filtering means, first channel filtering means, that

the feedback path of the feedback loop comprises second channel filtering means and that the product of the transfer function of the first channel filtering means and the transfer function of the second channel filtering means is constant.

Another embodiment of a receiver according to the invention which also has the possibility to independently design the channel filtering and the noise shaping is characterized by further combiner means with first and second inputs and an output, by a first filter with transfer function $F_1(s)$ connected between the output of the first mentioned combiner means and the first input of the further combiner means, a second filter with transfer function $F_2(s)$ connected between the output of the quantizer and the second input of the further combiner means and a third filter with transfer function $F_3(s)$ between the output of the further combiner means and the input of the quantizer, wherein the transfer function $F_1(s)/(F_1(s)+F_2(s))$ substantially corresponds with the frequency band of the communication channel to be filtered. When in this implementation the sum $F_1(s)+F_2(s)$ of the transfer functions of the first and second filters is equal to 1, these two filters, which are then complements of each other, perform together the channel filtering and the third filter does the noise shaping.

As is already observed earlier, one of the major objects of the present invention is to reduce the dynamic range of the signals generated by the analog to digital converter and consequently to reduce the complexity of the digital circuitry that has to process these signals. A further reduction of the dynamic range can be obtained by a properly designed automatic gain control and the receiver of the present invention may therefore be further characterized in that the feedback loop of the sigma-delta modulator comprises one or more gain controlled stages. The dynamic range may also be reduced by an AGC-stage in front of the ΣΔ-modulator but it may be advantageous to carry out the automatic gain control within the feedback loop of the ΣΔ-modulator because the stage is then to a lesser extent subject to large interferer signals so that the linearity requirements are less severe.

It may further be observed that the invention may be implemented with a time-continuous analog ΣΔ-modulator or with a time-discrete analog ΣΔ-modulator (a switched capacitance implementation). In the latter case an anti-aliasing low pass filter that suppresses all frequency components above half the sampling frequency, has to be placed prior to the ΣΔ-modulator.

It is noted that the present invention also relates to a sigma-delta modulator that is either fully or partly incorporated in a monolithic integrated circuit and which is intended for use in a receiver according to the invention.

The invention will be described with reference to the accompanying figs.. Herein shows:

Fig. 1 a receiver according to the invention with a first example of the sigma delta modulator used therein,

Fig. 2 a second example of a sigma delta modulator for use in a receiver according to the invention and

Fig. 3 a third example of a sigma delta modulator for use in a receiver according to the invention.

The receiver of fig. 1 comprises an amplifier A_1 that receives a band of communication channels from an antenna input. In a mixer M the amplified signals are mixed with a local oscillator frequency obtained from a tuned local oscillator O. In the arrangements to be described the oscillation frequency is equal to the carrier frequency of the desired channel, so as to transpose this channel to baseband (homodyne or zero-IF receiver), although the invention may also be used in a heterodyne receiver in which the desired communication channel is transposed to a suitable intermediate frequency signal. The output of the mixer M is again amplified in a second amplifier A_2 and subsequently applied to an analog to digital converter, which in this embodiment is constituted by a continuous time analog sigma-delta modulator SD. It may be observed that, in the arrangement of fig. 1, the signals X(s) applied to the sigma delta modulator are not or only scarcely filtered so that the desired baseband channel is accompanied by interfering neighbor channels (interferers), which may have amplitudes that are much larger than the amplitude of the desired baseband channel. Moreover the amplitude of this baseband signal is strongly dependent on the reception conditions so that the dynamic range of the input signals applied to the sigma delta modulator SD is very large.

The input signal X(s) to the ΣΔ-modulator is applied to a first combiner C_1 and the output signal thereof is applied to a first integrator I_1 with transfer function $1/s\tau_1$. The output signal of the first integrator is applied to a second combiner C_2 whose output is coupled to a second integrator I_2 with transfer function $1/s\tau_2$. The output signals of the second integrator are fed to a clocked quantizer Q that converts the analog signals to a series of digital words with the sample rate of the clock-frequency. The quantizer Q may generate

multi-bit words but conveniently the quantizer outputs single-bit words (bit-stream) in which case the quantizer may have the form of a one-level comparator. The output Y(z) of the quantizer is converted into analog pulses Y(s) in a digital to analog converter D and the analog pulses so obtained are applied through coefficient multipliers M_1 and M_2 with coefficients d_1 and d_2 to the combiners C_1 and C_2 respectively. In the arrangement of fig. 1 the combiners C_1 and C_2 are subtracters with respect to the signals from the multipliers M_1 and M_2 but it will be apparent that, when in the DA-converter D or in the multipliers M_1 and M_2 the polarity of the signal is reversed, the output signals of the multipliers have to be added in the combiners C_1 and C_2. The output signals of the second integrator I_2 are applied, through a third multiplier M_3 with coefficient b, to a further adding input of the combiner C_1.

The digital output bit-stream of the ΣΔ-modulator SD is fed to a decimation filter F for converting the bit-stream to multi-bit words of reduced sample rate. The output of the filter F may be processed in further digital circuitry (not shown). Moreover this output is applied to an automatic gain control stage B that controls the magnitude of the coefficients b, d_1 and τ_1 in respectively the units M_3, M_1 and I_1 of the ΣΔ-modulator.

In operation the input signal X(s) is low pass filtered by the low pass filter constituted by the two integrators I_1 and I_2 and the feedback of the analog pulses Y(s) through the multipliers M_1 and M_2. The usual function of a ΣΔ-modulator is to digitize the signal and to shift the quantization noise associated therewith to the higher frequency range (noise-shaping) between the frequency band of interest and half the sample (clock) frequency of the quantizer. Additionally the low pass filter of fig. 1 generates in the signal transfer of the ΣΔ-modulator a cut off frequency that approximately corresponds to the bandwidth of the desired channel, with the result that the desired channel is passed and the neighbor interferers are substantially suppressed and with the further result that the dynamic range of the signals within the feedback loop of the ΣΔ-modulator and thereafter is substantially reduced. In the arrangement of fig. 1 the signal transfer function of the ΣΔ-modulator, which is responsible for the channel filtering, is approximately $1/(s\,\tau_1 d_2+d_1)$, which is a low pass filter of 1st order.

The coefficient multiplier M_3 has substantially no effect on the channel filtering function of the ΣΔ-modulator but provides additional suppression of the quantization noise by implementing a local resonance close to the pass band of the desired signals.

A further substantial reduction of the dynamic range of the signals to be processed is obtained by automatic gain control. As already noted in the preamble to this patent application, this gain control can be performed inside the feedback loop of the ΣΔ-modulator as well as in front of the AD converter. In the arrangement of fig. 1 this is

implemented by equally varying the three coefficients d_1, τ_1 and b in the units M_1, I_1 and M_3 respectively. It can be shown that with this measure the gain of the arrangement is changed while the characteristic frequencies that are responsible for the channel filtering and the noise shaping remain unaffected.

Fig. 2 shows an alternative for the ΣΔ-modulator of fig. 1. In this arrangement the quantizer Q and the digital to analog converter D have the same function as the corresponding units of fig. 1. A combiner C_3 subtracts the feedback signal from the input signal X(s) and the difference signal is applied through a noise-shaping low pass filter G to the quantizer Q. The channel filtering is performed by a high pass filter H in the feedback path from the DA-converter to the combiner C_3 and by a low-pass filter L in cascade with the filter G. When the transfer function of the high pass filter H is H(s) and that of the low pass filter L is L(s) then the product H(s).L(s) is constant (i.e. frequency independent). For instance H(s).L(s) = 1.

When G(s) is the transfer function of the noise-shaping low pass filter G and when the combination of quantizer Q and digital to analog converter D is simulated by a linear amplifier with amplification A and a source of quantization noise ε, then the output signal Y(s) of the ΣΔ-modulator of fig. 2 can be expressed as:

$$Y(s) = X(s)\frac{A.G(s).L(s)}{1+A.G(s).L(s).H(s)} + \frac{\varepsilon}{1+A.G(s).L(s).H(s)}$$

With L(s).H(s) = 1 this becomes:

$$Y(s) = X(s)\frac{A.G(s).L(s)}{1+A.G(s).} + \frac{\varepsilon}{1+A.G(s).} .$$

From the first term of the right hand side of this equation it follows that, when the amplification A is sufficiently high, the signal transfer is substantially only dependent from the channel filter L (and its counterpart H) and from the second term it follows that the noise-shaping is only dependent from the noise-shaping filter G. Therefore the arrangement of fig. 2 allows optimizing the channel filtering and the noise-shaping independently from each other. The channel filtering is performed by proper dimensioning of the filters H and L, which may be of either first order or higher order or even band pass, and the noise-shaping is performed by proper dimensioning of the filter G which also may be of either first order or higher order or even band pass.

Fig. 3 shows another implementation of the ΣΔ-modulator. This arrangement has three filters F_1, F_2 and F_3 and an extra combiner C_4. The filter F_1 is placed between the output of the combiner C_3 and the positive input of the combiner C_4, The filter F_2 is placed

between the output of the DA converter D and the negative input of the combiner C_4 and the filter F_3 is connected between the output of combiner C_4 and the quantizer input. The unfiltered output of the DA-converter is fed to the negative input of the combiner C_3. If the filters F_1, F_2 and F_3 have the transfer functions L(s), H'(s) and G(s) respectively, the same formula for the signal Y(s) and the same advantages as given above apply, except in that the product L(s).H(s) is replaced by the sum L(s) + H'(s). The implementation of the channel filters H' can now be very simple, For instance, when L is a 1st order low pass RC-filter ($\tau = RC$) with transfer $L(s) = \frac{1}{s\tau + 1}$ the filter H' is an equally simple 1[st] order high pass RC-filter with transfer $H'(s) = \frac{s\tau}{s\tau + 1}$.

The arrangement of fig. 3 allows changing the implementation of the filters without changing the frequency characteristics of the ΣΔ-modulator as a whole. When for instance a differentiator with transfer function $s\tau$ is added to both the filters F_1 and F_2 and a compensating integrator with transfer function $1/s\tau$ to the filter F_3, then neither the channel filtering defined by $F_1(s)/(F_1(s) + F_2(s))$ nor the noise shaping, defined by $(F_1(s) + F_2(s))*F_3(s)$ is changed. With the above given transfer functions of L(s) and H'(s) the transfer functions of F_1, F_2 and F_3 are now respectively:

$$F_1(s) = s\tau.\frac{1}{s\tau + 1} = \frac{s\tau}{s\tau + 1},\ F_2(s) = s\tau.\frac{s\tau}{s\tau + 1} \text{ and } F_3(s) = \frac{1}{s\tau}.G(s)$$

In a further conversion step a single high pass section in F3 replaces the two high pass sections of F_1 and F2. This results in:

$$F_1(s) = 1,\ F_2(s) = s\tau,\ F_3(s) = \frac{1}{s\tau}.\frac{s\tau}{s\tau + 1}G(s) = \frac{1}{s\tau + 1}.G(s).$$

Therefore the filter F_1 is merely an interconnection, the filter F_2 is a differentiator and the filter F_3 is the original low pass filter G in series with a low pass filter section L. In all three cases the quotient $F_1(s)/(F_1(s) + F_2(s))$, that determines the channel filtering, is equal to $1/(s\tau + 1)$ and the product $(F_1(s) + F_2(s))*F_3(s)$ that determines the noise shaping, equals G(s). It may be observed that the multiplication factor τ of the differentiator determines the cut off frequency of the channel filter.

In the arrangements of figs. 2 and 3 gain control within the feedback loop of the ΣΔ-modulator is achieved by using a multiplying DA-converter D. When the quantizer Q delivers single-bit words, this DA-converter can be made very simple by means of a single current source that is AGC-controlled by the unit B and that is switched by the quantizer output pulses. When at higher levels of the input signal X(s) the current of this source is

increased, the feedback is increased with the result that the amplification of the ΣΔ-modulator is decreased.

The embodiments of the present invention described herein are intended to be taken in an illustrative and not a limiting sense. Various modifications may be made to these embodiments by those skilled in the art without departing from the scope of the present invention as defined in the appended claims.

It may be noted that the invention relates to homodyne receivers in which the desired channel is frequency-converted to baseband (zero-IF) as well as to heterodyne receivers with frequency-conversion of the desired channel to a suitable intermediate frequency band.

Although the embodiments discussed above primarely relate to receivers for wireless communication it will be clear to those skilled in the art that the invention may be applied advantageously in other receivers, for instance receivers as used in TV systems for receiving terrestrial satallite broadcasted TV signals, or TV signals broadcasted via cable networks.

CLAIMS:

1. A receiver comprising means for receiving a plurality of communication channels, a mixer (M) for frequency-converting at least part of said communication channels and a sigma-delta modulator (SD) for analog to digital converting output signals of the mixer, said sigma-delta modulator including a feedback loop with a forward path and a feedback path, wherein the forward path comprises combiner means (C_3) with a first input receiving the mixer output signals, noise-shaping low pass filtering means (G) coupled to the output of said combiner means and a quantizer (Q) coupled to the output of the noise-shaping low pass filtering means and wherein the feedback path is connected to supply output signals of the quantizer (Q) to a second input of the combiner means (C_3), characterized in that the forward path and the feedback path are so arranged that the signal transfer function of the $\Sigma\Delta$-modulator has a pass band that substantially corresponds with the frequency band of the communication channel to be filtered while the interferers beyond that pass band are attenuated.

2. A receiver as claimed in claim 1 characterized in that the forward path of the feedback loop comprises, in addition to said noise shaping low pass filtering means (G), first channel filtering means (L), that the feedback path of the feedback loop comprises second channel filtering means (H) and that the product of the transfer function of the first channel filtering means and the transfer function of the second channel filtering means is constant.

3. A receiver as claimed in claim 1 characterized by further combiner means (C_4) with first and second inputs and an output, by a first filter (F_1) with transfer function $F_1(s)$ connected between the output of the first mentioned combiner means (C_3) and the first input of the further combiner means (C_4), a second filter (F_2) with transfer function $F_2(s)$ connected between the output of the quantizer (Q) and the second input of the further combiner means (C_4) and a third filter (F_3) with transfer function $F_3(s)$ between the output of the further combiner means (C_4) and the input of the quantizer (Q), wherein the transfer function $F_1(s)/(F_1(s)+F_2(s))$ substantially corresponds with the frequency band of the communication channel to be filtered.

4. A receiver as claimed in any of the preceding claims characterized in that the sigma-delta modulator comprises one or more gain controlled stages (M_1, I_1, M_3, D).

5. A sigma delta modulator specifically intended for use in a receiver as claimed in one or more of the preceding claims.

ABSTRACT:

In a receiver receiving a plurality of signal channels analog to digital conversion is done by a $\Sigma\Delta$-modulator. The filtering of the desired signal channel is positioned within the feedback loop of the $\Sigma\Delta$-modulator.

Fig. 2

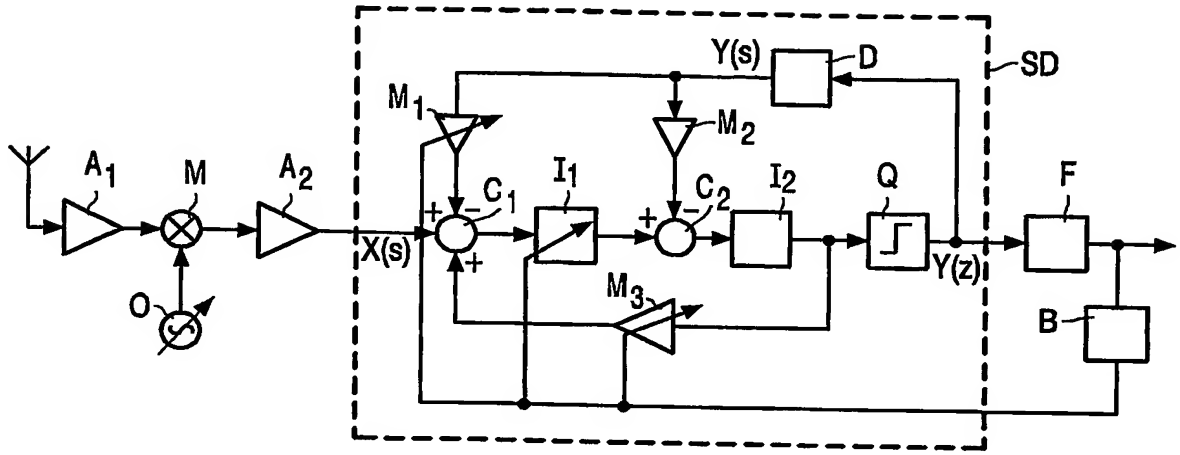

FIG. 1

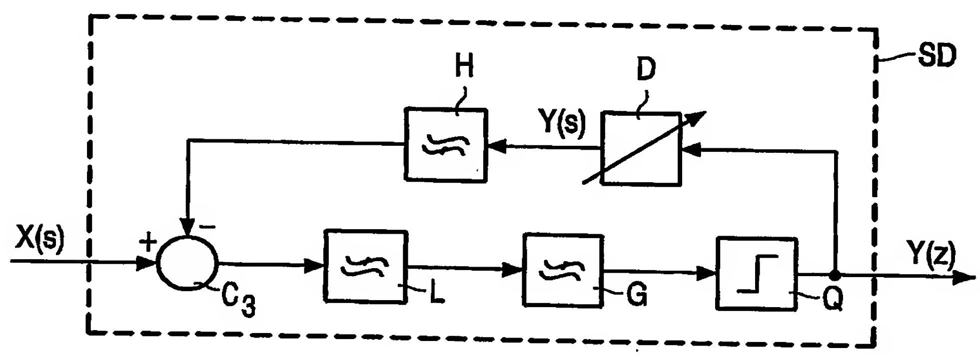

FIG. 2

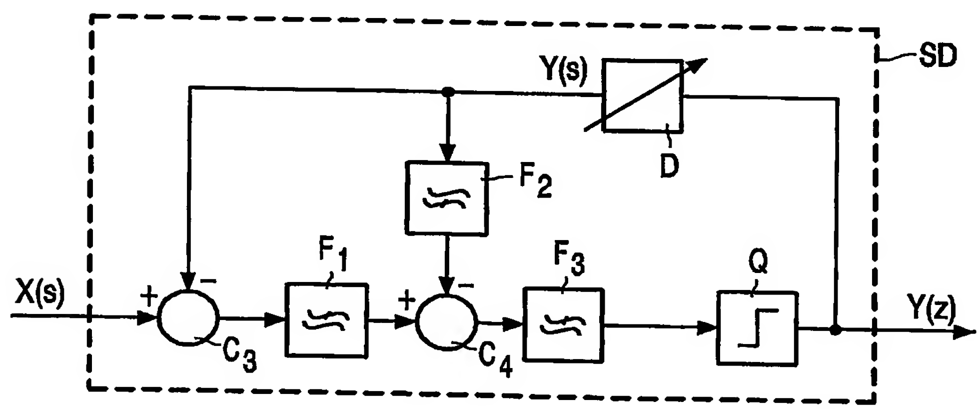

FIG. 3

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